Electronic Version
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Claims

[c1] 1. A complementary metal oxide semiconductor (CMOS) transistor, comprising:
a first thin-film transistor (TFT) of a first conductivity type, comprising:
a first gate; and
a first polysilicon island under the first gate, comprising:
a first channel region right under the first gate;
a source region on one side of the first gate; and
a first doped region of a first conductivity type on the other side of the first gate, wherein the source region, the first channel region and the first doped region are arranged along a first direction;
a second TFT of a second conductivity type, comprising:
a second gate; and
a second polysilicon island under the second gate, comprising:
a second channel region right under the second gate;
a second doped region of a second conductivity type on one side of the second gate; and
a drain region on the other side of the second gate, wherein the second doped region, the second channel region and the drain region are arranged along the first

direction, and the second doped region and the first doped region of the first TFT are arranged along a second direction that is perpendicular to the first direction;
an inter-layer dielectric layer covering the first TFT and the second TFT, having a plurality of contacts therein connecting with the first doped region and the second doped region, respectively;
a conductive line on the inter-layer dielectric layer extending along the second direction, the conductive line electrically connecting the first doped region and the second doped region via the contacts;
a source contact metal disposed on and through the inter-layer dielectric layer to electrically connect with the source region; and
a drain contact metal disposed on and through the inter-layer dielectric layer to electrically connect with the drain region.

[c2] 2. The CMOS transistor of claim 1, wherein the first TFT comprises a low-temperature polysilicon (LTPS) TFT.

[c3] 3. The CMOS transistor of claim 1, wherein the second TFT comprises a LTPS TFT.

[c4] 4. The CMOS transistor of claim 1, wherein the first TFT comprises an N-type TFT.

[c5] 5. The CMOS transistor of claim 4, wherein the first polysilicon island further comprises a lightly doped drain (LDD) region between the first channel region and the source region as well as between the first channel region and the first doped region.

[c6] 6. The CMOS transistor of claim 4, wherein the second TFT comprises a P-type TFT.

[c7] 7. The CMOS transistor of claim 1, wherein the first TFT comprises a P-type TFT.

[c8] 8. The CMOS transistor of claim 7, wherein the second TFT comprises an N-type TFT.

[c9] 9. The CMOS transistor of claim 8, wherein the second polysilicon island further comprises a lightly doped drain (LDD) region between the second channel region and the drain region as well as between the second channel region and the second doped region.

[c10] 10. A CMOS-based device, comprising:
at least one first LTPS TFT of a first conductivity type, comprising:
a first gate line; and
a first polysilicon island under the first gate line, comprising:
a first channel region right under the first gate line;

a first doped region on one side of the first gate line; and

a second doped region on the other side of the first gate line;

a plurality of second LTPS TFTs of a second conductivity type arranged parallel to the first LTPS TFT, wherein each second LTPS TFT comprises:

a second gate line; and

a second polysilicon island under the second gate line, comprising:

a second channel region right under the second gate line;

a third doped region on one side of the second gate line; and

a source/drain region on the other side of the second gate line;

an inter-layer dielectric layer covering the first TFT and the second TFT, having a plurality of contacts therein connecting with the first doped region, the second doped region and the third doped region, respectively;

a plurality of conductive lines on the inter-layer dielectric layer extending substantially parallel to the first gate line and the second gate line, wherein one conductive line electrically connects the first doped region and the third doped region via a set of the contacts, and another conductive line electrically connects the second doped

region and the third doped region via another set of the contacts; and

a plurality of source/drain contact metals disposed on and through the inter-layer dielectric layer, wherein each source/drain region is connected with at least one source/drain contact metal.

[c11] 11. The CMOS-based device of claim 10, wherein the second TFTs comprise P-type TFTs.

[c12] 12. The CMOS-based device of claim 11, wherein the first TFT comprises an N-type TFT.

[c13] 13. The CMOS-based device of claim 12, wherein the first polysilicon island further comprises a lightly doped drain region between the first channel region and the first doped region as well as between the first channel region and the second doped region.